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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RILEY, SHAWN	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,153	GIANDALIA ET AL.	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Oct 2003 filing*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-14 and 16* is/are rejected.

7)☒ Claim(s) *6-8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawing(s) is(are) objected to because they fail to label (figure(s) 2A & 2B where Vin is from in figure 2B, what is Vi in figure 2A and also what is the output node in figure 2A—Vin?) and further labeling of the boxes 17 in figure 1 and 7 in figure 2A to help determine what the element boxes are. Without some indication as to the content of the boxes (or preferably ansi symbols of the actual elements) it is not clear as to what the elements are and they are not explanatory to a reader as a quick method of determining the general background of the invention.

See MPEP 608.02 subparagraph (o) -- **Legends**

> Suitable descriptive legends may be used, or may be required by the Examiner, where necessary for understanding of the drawing, subject to approval by the Office. They should contain as few words as possible.

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-5, 10, and 12-13 are rejected under 35 U.S.C. §102(b) as being fully anticipated by Ishikawa et al. (U.S. Patent 5,619,403). Ishikawa et al show,[1] (in, e.g., the(ir) figures 18 and corresponding disclosure)

As to claim 1;

A switch mode power supply (see, e.g., figure 18) for supplying an output voltage and current to a load, comprising: a transformer including a primary winding (T1) and a secondary winding; a primary circuit comprising a switching stage (that is how a transformer works, i.e., a switching stage is connected at some point forward of the transformer) electrically coupled to the primary winding of the transformer; and a secondary circuit connected to the secondary winding of the transformer, wherein the secondary circuit comprises a rectifier circuit (D1) electrically coupled on an input side to the secondary winding, the rectifier circuit providing a rectified output voltage to a storage capacitor (C2), and an output circuit including a switching device (Tr2) electrically connected on one side of the switching device to the rectifier circuit and on another side of the switching device to one side of an output capacitor, an output terminal

1 Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material. For method claims, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the apparatus will not be repeated.

and an input of a voltage sensing and control circuit(R3/R4/Q1), and the voltage sensing and control circuit providing an output (D/Dr3) that controls switching of the switching device such that the output voltage is regulated.

As to claim 2;

The power supply of claim 1, wherein the output circuit does not comprise an inductor (as described above vis a vis the output circuit, no inductor is described).

As to claim 4;

The power supply of claim 3, wherein the voltage sensing and control circuit comprises a resistor divider (R3/R4) electrically connected across the output capacitor and having a node electrically connected to a comparator (Q1) , and the comparator compares a voltage at the node to a reference voltage (R5/R6) and is operably connected to the gate of the field effect transistor (through Tr3 and R2) such that field effect transistor is switched on and off regulating the output voltage.

As to claim 5 (see rejection of claim 4);

The power supply of claim 1, wherein the voltage sensing and control circuit comprises a resistor divider electrically connected across the output capacitor and

having a node electrically connected to a comparator, and the comparator compares a voltage at the node to a reference voltage and is operably connected to the switching device, such that the switching device regulates the output voltage.

As to claim 10 (see, in part, rejection of claim 11);

The power supply of claim 1, wherein the transformer comprises a planar isolation transformer (i.e., based on the fact the circuitry is placed onto an ic, see, e.g., figure 22 and disclosure thereof, the transformer is a planar isolation transformer).

As to claim 12 (see rejection of claim 1);

An output circuit for a step-down converter, the step-down converter having an output voltage across a first lead and a second lead, the output circuit comprising:

a switching device electrically connected on one side of the switching device to the first lead and on another side of the switching device to one side of a capacitor, an output terminal and an input of a voltage sensing and control circuit, wherein the voltage sensing and control circuit is operably connected to the switching device such that the switching device regulates the output voltage of the step-down converter, the voltage sensing and control circuit switching the switching device on when the output voltage drops below a reference voltage.

As to claim 13 (see rejection of claim 2);

The output circuit of claim 12, wherein an inductor is not coupled in the output circuit.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 3, 14, and 16 are rejected under 35 U.S.C. § 103 as being unpatentable over by Ishikawa et al. The by Ishikawa et al reference discloses the limitations of the invention as claimed as described above. However, by Ishikawa et al do not show the switch as a MOSFET/FET and instead shows a bipolar transistor. Official notice is taken that it would have been obvious at the time the invention was made to utilize the switch as a MOSFET/FET and instead shows a bipolar transistor into the circuit of Ishikawa et al for the reason of providing an equivalent switching function. That is, many varieties of bipolar transistors and FETs exist and are designed for equivalent and at times different environments. For instance, some bipolar transistors are able to withstand a higher reverse breakdown voltage which is generally traded for a slower switching speed. These various types of similar transistors (e.g., pnp and npn bipolar

transistors with wider channels, different amounts of doping, or MOSFETs, IGBTs, etc.) have in common the use of providing a desired transresistance function (by current for bipolars). Accordingly, it would have been obvious to one of ordinary skill in the art to replace bipolar transistors with a MOSFET/FET given the expected working environment in view of their closely related theoretical basis (all pass transistors in general) and the resulting expectation of a similar result, i.e., providing a current pass function by current for a bipolar (or likewise providing a current pass function by voltage for an FET).

Claim 9 is rejected under 35 U.S.C. § 103 as being unpatentable over by Ishikawa et al. The Ishikawa et al reference discloses the limitations of the invention as claimed as described above. However, Ishikawa et al does not show a voltage doubler on the secondary. Official notice is taken that it would have been obvious at the time the invention was made to utilize a voltage doubler into the circuit of Ishikawa et al for the reason of a design choice wherein, e.g., an output of twice the voltage for providing power to a high voltage load would require a voltage doubler, and conversely, where a high voltage load is required, and to not use a voltage doubler where a load requires half the voltage output level.

Claim 11 is rejected under 35 U.S.C. § 103 as being unpatentable over by Ishikawa et al. The Ishikawa et al reference discloses the limitations of the invention as claimed as described above. However, Ishikawa et al does not show providing for the planar primary and the secondary windings to be on opposite sides of the printed circuit board. It would have been obvious at the time the invention was made to utilize planar primary and the secondary windings on opposite sides of the printed circuit board into the circuit of Ishikawa et al for the reason of design choice. That is with limited space on a single side of a ic, utilizing the obverse would allow for a compact size vis a vis utilizing only a single size of an ic.
As to claim 11;

As to claim 11;

The power supply of claim 10, wherein the planar isolation transformer comprises a printed circuit board transformer (at column 16 lines 17-25, reffering to FIG. 22, Ishikawa et al. show a diagram illustrating the use of a one-chip IC design, so that the apparatus can be provided in a small size and can be used for general purposes) comprising the primary winding and the secondary winding deposited on opposite sides of a printed circuit board.

Allowable Subject Matter

5. Claims 6-8 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P.

7. The following is an examiner's statement of reasons for allowance: No prior art uncovered anticipates or renders obvious applicant(s) claimed control circuit including a hysteretic comparator and the hysteretic comparator compares a voltage related to the output voltage with a reference voltage such that the output voltage sensing and control circuit turns the field effect transistor on and off regulating the output voltage. Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed primary circuit including a resistor divider electrically connected across a DC blocking capacitor, the

resistor divider having a node, the node being electrically connected to a comparator such that a second switching device and a third switching device are alternatingly switched on and off at a frequency determined by an oscillator.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

January 05

Shawn Riley
Primary Examiner